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Possible applications of nanoscale CMOS are examined, with a view to better defining the likely capabilities of future microelectronic systems. This analysis covers both data processing applications and nondata processing applications such as RF and imaging. Finally, we speculate on the future of CMOS for the coming 15 – 20 years.

Nanoscale CMOS - Proceedings of the IEEE

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are scaled down into the nanometer range, a number of major nonidealities must be addressed and overcome to achieve a successful analog and physical circuit design.

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Nanoscale CMOS Abstract: This paper examines the apparent limits, possible extensions, and applications of CMOS technology in the nanometer regime. Starting from device scaling theory and current industry projections, we analyze the achievable performance and possible limits of CMOS technology from the point of view of device physics, device technology, and power consumption.

Nanoscale CMOS - IEEE Journals & Magazine

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Nanotechnology promises to open up new ways of scaling CMOS circuits by introducing new materials. For example, a hybrid circuit of CMOS gates and carbon nano-tubes (CNT), NEMS relay logic and emerging memory devices have been proposed for future nano-scale Field Programmable Gate Arrays (FPGAs).

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Google Scholar Cross Ref Steven Hsu, et al., "A 280mV-to-1.1V 256b reconfigurable SIMD vector permutation engine with 2-dimensional shuffle in 22nm CMOS," Solid-State Circuits Conference ...

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Three-Dimensional Nanoscale Mapping of State-of-the-Art Field-Effect Transistors (FinFETs) - Volume 23 Issue 5 - Pritesh Parikh, Corey Senowitz, Don Lyons, Isabelle Martin, Ty J. Prosa, Michael DiBattista, Arun Devaraj, Y. Shirley Meng

Three-Dimensional Nanoscale Mapping of State-of-the-Art ...

Abstract: Steep subthreshold swing transistors based on interband tunneling are examined toward extending the performance of electronics systems. In particular, this review introduces and summarizes progress in the development of the tunnel field-effect transistors (TFETs) including its origin, current experimental and theoretical performance relative to the metal-oxide-semiconductor

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field ...

Low-Voltage Tunnel Transistors for Beyond CMOS Logic ...

ABSTRACT CMOS technology scaling has followed Moore's law well into the nano-scale regime now. The technology scaling is no longer just about geometric reduction but more about innovation in the use of new materials and transistor architectures.

Circuit Design in Nano-Scale CMOS Technologies ...

Nanoscale Cmos Proceedings Of The nanoscale CMOS are examined, with a view to better defining the likely capabilities of future microelectronic systems. ... PROCEEDINGS OF THE IEEE, VOL. 87, NO. 4, APRIL 1999 537. Table 1 Technology Scaling Rules for Three Cases (  $L$  is the Dimensional Scaling Parameter,  $L_{ns}$  is the Nanoscale CMOS

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- Proceedings of the IEEE

Nanoscale Cmos Proceedings Of The Ieee - Aplikasi Dapodik  
ICCAD '05: Proceedings of the 2005 IEEE/ACM International  
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FinFETs for nanoscale CMOS digital integrated circuits ...  
Electronics, an international, peer-reviewed Open Access journal.  
Dear Colleagues, CMOS technology will continue to expand its  
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Abstract: As complementary metal-oxide-semiconductor (CMOS) technologies are scaled down into the nanometer range, a number of major nonidealities must be addressed and overcome to achieve a successful analog and physical circuit design. The nature of these nonidealities has been well reported in the technical literature.

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